In the Claims

Please amend the claims as follows.

1. (Previously Presented) A method of handling register spills in a CPU having parallel registers, said parallel registers including a first register set and a second register set, the method comprising:

   (i) determining that register spill instructions in spill code generated by a register allocator can be paired, wherein paired register spill instructions relate to corresponding register locations in each of the first register set and the second register set and that no instructions between said register spill instructions modify any of said register spill instructions;

   (ii) based on the determining, modifying said register spill instructions as a parallel register spill instruction; and

   (iii) based on said modified parallel register spill instruction, configuring storage of associated register spills in memory in such a manner that said register spills can be loaded into said first and second register sets in parallel, wherein the configuring includes allocating space on a memory stack such that paired register spills are double word aligned.

2. (Cancelled)

3. (Previously Presented) The method of claim 1, wherein (i) includes determining that said register spill instructions are in a basic block within said spill code.

4. (Cancelled)

5. (Cancelled)

6. (Previously Presented) The method of claim 2, wherein (iii) includes allocating space on said memory stack for any remaining register spills.

7. (Cancelled)

8. (Previously Presented) The method of claim 1, further comprising loading said paired register spills from said memory stack back into corresponding register locations in each of said first register set and said second register set in parallel.

9-23. (Cancelled)